CINEC CAMPUS
Beyond A Graduate

CINEC Campus
Faculty of Engineering & Technology
Department of Electrical & Electronic Engineering
BSc Hons (Eng) Automotive, Mechanical, Civil, Mechatronics, Electronic & Telecommunication Engineering
Semester 3 / First Sit / Written Exam / 2025

Module Code	:	**FE2313**
Module Title	:	**Engineering Profession**
Date	:	**24th Feb 2025**
Examiner	:	**Eng. Wipula Wimalshanthi**
Time Allowed	:	**03 hrs.**

INSTRUCTIONS TO CANDIDATES

- This is a **closed book** examination.
- This paper consists of **04 descriptive type questions**. You Should Answer **ALL** questions.
- Write clearly legibly with a blue or black pen.
- Use only the **CINEC Answering Booklet**. Additional sheets may be requested from the invigilators.
- This paper contains **03** pages.

Question 1 [25 Marks]

1.1) Briefly describe the roles of following categories of personnel who are identified as members of the Technology Team.

i. Scientist

ii. Engineer

iii. Technician

[10 Marks]

1.2) Identify five (05) major engineering challenges that the world is facing today and describe each of these challenges with real world examples.

[15 Marks]

Question 2 [20 Marks]

2.1) Breifly describe why 'Soft Skills' are essential for practicing engineers?. [05 Marks]

2.2) Name six (06) essential soft skills that should be possessed by engineers.[07 Marks]

2.3) State the steps to be taken in Engineering Problem Solving. [08 Marks]

Question 3 [25 Marks]

3.1) Briefly describe the following;

i. Risk (Typical dictionary definition)

ii. Risk appetite

iii. Risk culture

iv. Risk thermostat

[08 Marks]

3.2) Most common way of assessing risk is risk mapping through an impact / likelihood matrix. Draw a 3 x 3 Risk Map indicating `Possible', `Probable' and `Remote' Likelihood levels and `Low', `Medium' and `High' Impact levels and identify the risk area where immediate mitigation action is required and the risk area where no mitigatory action is needed.

[05 Marks]

3.3) What is the standard definition for "Project"? Discuss the meaning of key words used.

[05 Marks]

3.4) What are the main responsibilities of a Project Manager?
[Write down at lease 06 responsibiliries]

[07 Marks]

Question 4 [30 Marks]

Case study:

Peter has been working as a project engineer for an energy technology company for a few years now, and has recently been promoted to review projects for communities with financial difficulties. He has been put in charge of managing the current company's charity projects, and determining how to distribute the funding for them.

Some of the projects are pretty straightforward in their mission and material requirement, but for one project, Peter isn't sure whether the company should be funding it. The project's mission is to provide new Solar Panels for a community experiencing financial difficulties, but the project data suggests it is more practical to just install better lighting inside the homes. Peter wonders whether to bring up his doubts with his boss. Based on the company's research on the community, the community desires better lighting system for their homes, and the Solar Panels would be an expensive and high maintenance project. Not to mention, there was a previous project that (when followed through) resulted in equipment being stolen from the same region to exchange for money.

Peter understands their local sponsor would gain a great advantage in featuring solar panels in the community. It would also foster a good business partnership between the two companies. However, Jack feels it is his responsibility to provide the community with a more simple and efficient solution to their problem, without diving into a large project that could possibly lead to negative side effects.

i. Should Jack discuss this matter with his boss? Elaborate your answer with reasoning.

ii. Discuss the advantages and drawbacks in proceeding with the Solar panel project.

iii. Is Jack's company wrong to provide technology to the community when they don't need it?

[Your combine answers to (i), (ii) and (iii) above shall not be less than 500 words.]

Disclaimer: The case given above is totally fictitious and has no relation to any organizations or living / deceased persons.

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BSc Hons (Eng) Electronic and Telecommunication Engineering
BSc Hons (Eng) Mechanical Engineering
Semester 03 First-Sit Examination 2025

Module Code : **EE2314**
Module Title : **Analogue Electronics**
Date : **18th February 2025**
Examiners : **Ms. Dushani Munasinghe**
Time Allowed : **9.00AM – 12.00PM; 03hrs**

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MATERIALS REQUIRED

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Question 01

(a) Discuss how the placement of *operating point (Q-point)* on the DC load line affects the transistor acting as an amplifier.
[*Give at least three (03) points to justify your answer*]

[03 Marks]

(b) A *silicon-based NPN bipolar junction transistor (BJT)* used in a common-emitter amplifier configuration is shown in Figure 1. It has a supply voltage (V_{CC}) of $12V$. The base resistor (R_B) is $240k\Omega$, and the collector resistor (R_C) is $2.2k\Omega$. Given that the transistor has a current gain (β) of 50 and a base-emitter voltage (V_{BE}) of $0.7V$, determine:

(i) The DC operating point (Q-point), (I_{BQ}, I_{CQ}, V_{CEQ}).

(ii) Sketch the DC load line and mark the Q-point on the load line.

(iii) Find $I_E, V_{BC}, V_C, V_B, V_E$.

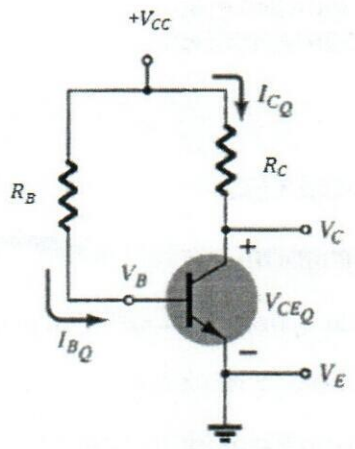

Figure 1

[16 Marks]

(c) Assume that current gain (β) for the transistor configuration in part (ii) is increased by 50% due to the effect of the change in temperature.

(i) Determine the new values of I_C and V_{CE} for the transistor configuration in part (ii).

(ii) Compare the change in I_C and V_{CE} because of the variation of β and propose a new biasing configuration which is less sensitive to temperature changes.

[06 Marks]

[Total - 25 Marks]

Question 02

(a) Explain briefly, highlighting the role of *AC analysis*, the benefits of small-signal modeling, and its importance in designing and analyzing transistor-based amplifiers.

[03 Marks]

(b) Consider the r_e model (small signal AC equivalent circuit) shown in Figure 2, for a voltage divider bias configuration. If $R_1 = 39k\Omega$, $R_2 = 4.7k\Omega$, $R_C = 3.9k\Omega$, $R_E = 1.2k\Omega$, $\beta = 100$, $r_o = 50k\Omega$ with a DC supply voltage of $V_{CC} = 16V$,

(i) Determine r_e

(ii) Calculate Z_i

(iii) Calculate $Z_o(r_o = \infty\Omega)$

(iv) Find $A_v(r_o = \infty\Omega)$

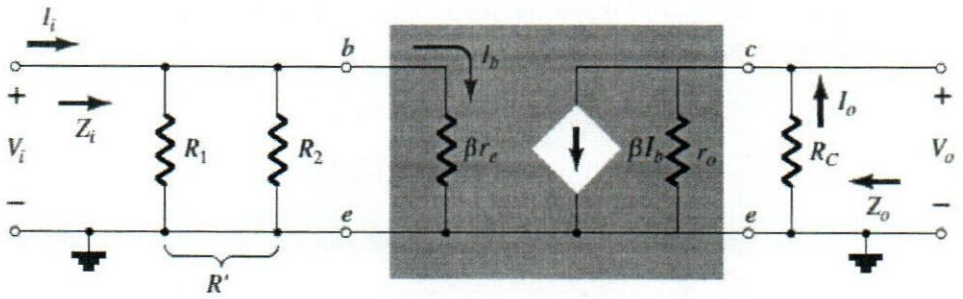

Figure 2

[16 Marks]

(c) A *2N3904 NPN transistor* is used in a common-emitter amplifier configuration. The transistor has the following small-signal parameters at $V_{CE} = 10V$, $I_C = 1mA$, and operating frequency, $f = 1kHz$:

- Input Impedance: $h_{ie} = 1.0k\Omega$
- Reverse Voltage Transfer Ratio: $h_{re} = 0.5 \times 10^{-4}$
- Forward Current Gain: $h_{fe} = 100$
- Output Admittance: $h_{oe} = 40\mu s$

Calculate the voltage gain (A_v) of the amplifier using h-parameter model.

[06 Marks]

[Total - 25 Marks]

Question 03

(a) Consider a differential amplifier with two inputs and two outputs,

(i) Discuss the significance of common-mode operation in differential amplifier configurations, particularly in terms of *common-mode rejection ratio (CMRR)*.

(ii) If a differential amplifier has a differential gain (A_d) of 1000 a common-mode gain (A_{CM}) of 8, calculate its CMRR (in dB).

[07 Marks]

(b) Consider an ideal operational amplifier,

(i) Explain the concept of *"virtual ground"* of an op-amp by considering an inverting amplifier circuit with negative feedback.

(ii) Consider an inverting amplifier (with a fixed resistor, $R_1 = 10k\Omega$, a variable resistor, $R_2 = 10k\Omega$ and a feedback resistor, $R_f = 500k\Omega$) with negative feedback as shown in Figure 3. Calculate the range of voltage gain ($A_v = V_o/V_i$) of this amplifier circuit.
[*Hint: Consider the variable resistor ranging the value from* $0k\Omega$ *to* $10k\Omega$ *when calculating the range of the voltage gain.*]

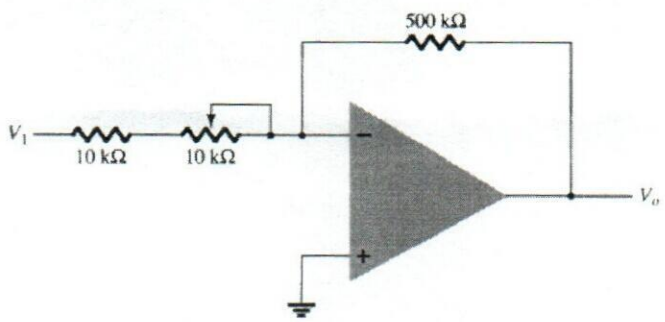

Figure 3

[11 Marks]

(c) An inverted summing amplifier (op-amp-based adder) is used in an audio mixing circuit, where multiple input signals are combined into a single output. The circuit operates with a dual power supply of $\pm 12V$ and has the following parameters:

- Input resistors: $R_1 = 10k\Omega$, $R_2 = 20k\Omega$, $R_3 = 30k\Omega$
- Feedback resistor: $R_f = 40k\Omega$
- Input signals: $V_1 = 1V$, $V_2 = 2V$, $V_3 = 3V$

Calculate V_{out} for the given circuit parameters.

[07 Marks]

[Total - 25 Marks]

Question 04

(a) Power amplifiers are classified based on their operating conditions and conduction cycles.

(i) Define and differentiate the Class A, Class B, Class AB and Class C power amplifiers.

(ii) Discuss the cause of *"crossover distortion"* in class B push-pull configuration using an appropriate illustration. Suggest a method to minimize crossover distortion.

[08 Marks]

(b) Consider the series-fed class A power amplifier circuit shown in Figure 4 with the circuit parameters, $V_{CC} = 20V$, $R_C = 10\Omega$, and $I_{CQ} = 1A$.

(i) Calculate the input dc power ($P_i(dc)$) and the output ac power ($P_o(ac)$).

(ii) Find the amplifier efficiency based on the answers you obtained for part (a).

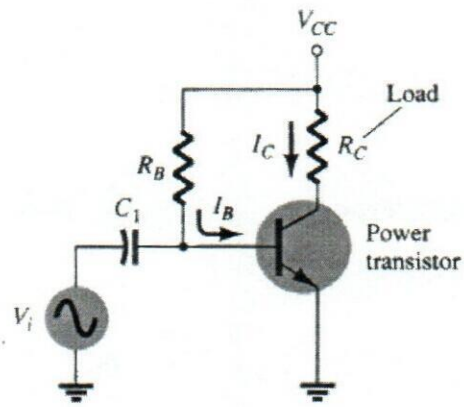

Figure 4

[14 Marks]

(c) Operational amplifier (op-amp) circuits can be designed using both negative feedback and positive feedback. While negative feedback stabilizes the circuit and allows the op-amp to function as an amplifier, positive feedback forces the circuit to operate as a comparator or an oscillator. Sketch an op-amp circuit with positive feedback based on your knowledge on op-amps.

[03 Marks]

[Total - 25 Marks]

FORMULA SHEET

Bipolar Junction Transistors

DC Biasing

$$I_C = \beta I_B \ ; \ V_{BE} = V_B - V_E \ ; \ V_{CE} = V_C - V_E \ ; \ V_{BC} = V_B - V_C$$

BJT small-signal modelling (r_e model)

Approximate analysis of voltage divider bias,

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} \ ; \ V_E = V_B - V_{BE} \ ; \ I_E = \frac{V_E}{R_E}$$

$$r_e = \frac{26mV}{I_E}$$

$$R' = R_1 \parallel R_2 = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$Z_{in(base)} = \beta r_e$$

$$Z_i = R' \parallel Z_{in(base)}$$

For $r_o \to \infty$, we approximate:

$$Z_o = R_C \ ; \ A_v = -\frac{R_C}{r_e}$$

Voltage gain of h-parameter model:

$$A_v = -\frac{h_{fe} R_C}{h_{ie} + (1 + h_{fe}) R_E}$$

Operational Amplifiers

$$CMRR = \frac{A_d}{A_{CM}}$$

$$A_v = -\frac{R_f}{R_{in}}$$

Power Amplifiers

Input DC power and output AC power:

$$P_{i(dc)} = V_{CC} \times I_{CQ} \ ; \ P_{o(ac)} = \frac{I_{CQ}^2 \times R_C}{2}$$

Power amplifier efficiency:

$$\eta = \left(\frac{P_{o(ac)}}{P_{i(dc)}} \right) \times 100\%$$

-END OF EXAMINATION PAPER-

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Semester 03 First-Sit Examination 2025

Module Code	**: EE2314**
Module Title	**: Analogue Electronics**
Date	**: 18th February 2025**
Examiners	**: Ms. Dushani Munasinghe**
Time Allowed	**: 9.00AM – 12.00PM; 03hrs**

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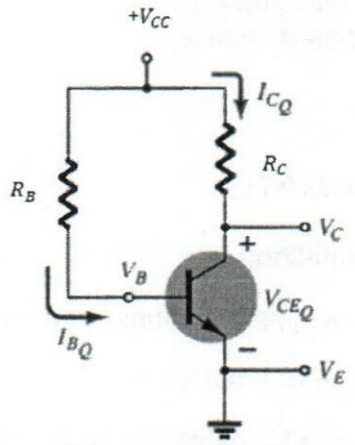

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(b) Consider the r_e model (small signal AC equivalent circuit) shown in Figure 2, for a voltage divider bias configuration. If $R_1 = 39k\Omega$, $R_2 = 4.7k\Omega$, $R_C = 3.9k\Omega$, $R_E = 1.2k\Omega$, $\beta = 100$, $r_o = 50k\Omega$ with a DC supply voltage of $V_{CC} = 16V$,

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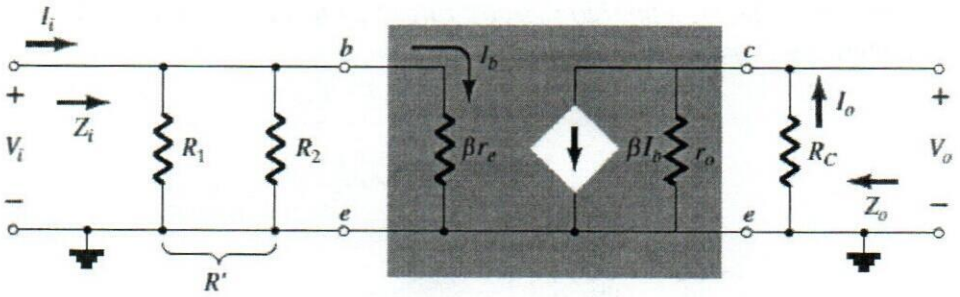

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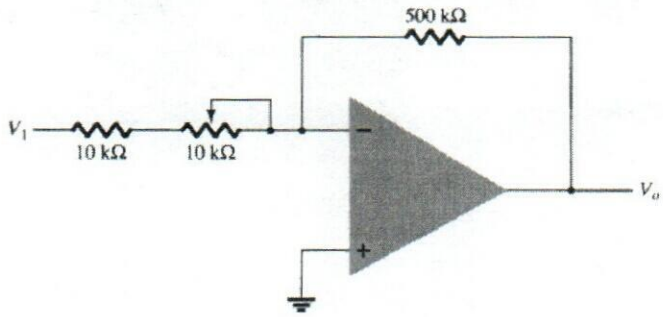

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Calculate V_{out} for the given circuit parameters.

[07 Marks]

[Total - 25 Marks]

Question 04

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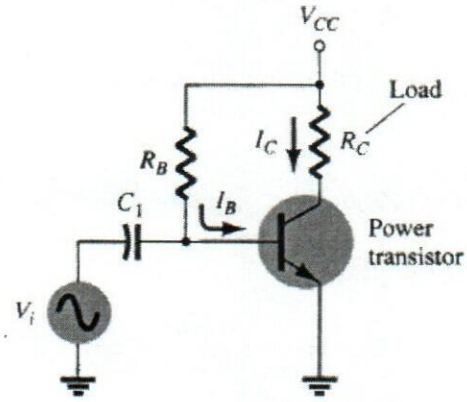

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Semester 05 First-Sit Examination 2025

Module Code : **EE3317**
Module Title : **Electromagnetics**
Date : **29th January 2025**
Examiners : **Ms. Dushani Munasinghe**
Time Allowed : **1.30PM – 4.30PM; 03hrs**

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Question 01

(a) Electrostatics studies about electric fields created due to stationary charges while magnetism reveals about magnetic fields created by magnets or moving charges. State Gauss's law for electrostatics and Ampere's law for magnetism along with differential forms of Maxwell's equations that describes them mathematically.

(06 Marks)

(b) Determine the total charge on the line, $0 < x < 5(m)$ if the line charge density, $\rho_L = 12x^2 mC/m^2$.

(07 Marks)

(c) Consider two conducting plates shown in Figure 1. If $V(z = 0) = 0V$ and $V(z = 2mm) = 50V$, determine the electric potential, V, electric field intensity, $\vec{E}$ and electric flux density, $\vec{D}$ in the dielectric region where, relative permittivity, $\epsilon_r = 1.5$ between the plates.

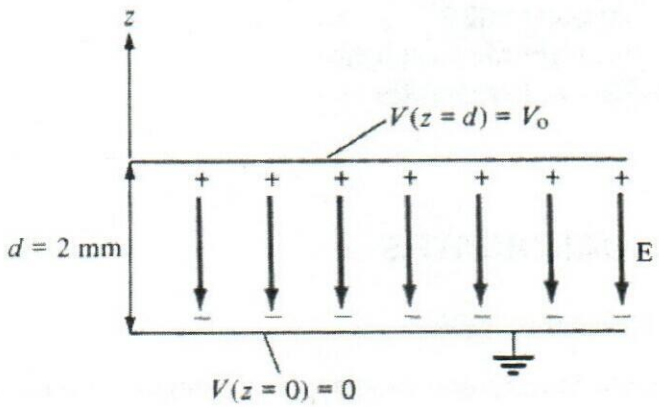

Figure 1

(12 Marks)

[Total - 25 Marks]

Question 02

(a) Dynamic electric fields are governed by Faraday's law and dynamic magnetic fields are governed by Ampere's circuit law with Maxwell's correction by adding the displacement current. State Faraday's and Ampere's laws and express them in their differential forms of Maxwell's equations.

(06 Marks)

(b) Time-harmonic fields are electromagnetic wave fields that vary sinusoidally with time at a fixed frequency. Consider the time-harmonic field given in equation (1).

$$\vec{E} = 10cos(10^8 t - 5x + 30^0)\hat{a}_z \quad (1)$$

(i) State the direction of oscillation of the electric field.

(ii) State the direction of propagation of the electromagnetic wave.

(iii) Express the time-harmonic field given in equation (1) in phasor form.

(06 Marks)

(c) In a medium characterized by $\sigma = 0, \mu = \mu_0$ and $\epsilon = 4\epsilon_0$, the electric field (in V/m) is expressed in equation (2). Calculate β and $\vec{H}$.

$$\vec{E} = 20cos(10^8 t + \beta z)\hat{a}_y \quad (2)$$

(13 Marks)

[Total - 25 Marks]

Question 03

(a) Calculate the phase constant, β for a $15.9MHz$ uniform plane wave travelling in free space where, wave propagation happens at the speed of light ($c = 3 \times 10^8 ms^{-1}$).

(05 Marks)

(b) A uniform plane wave propagating in a good conductor has the electric field (V/m) expressed in equation (3). If the medium is characterized by $\epsilon_r = 1, \mu_r = 20$ and $\sigma = 3S/m$, find α, β and $\vec{H}$.

$$\vec{E} = 2e^{-\alpha z} cos(10^8 t + \beta z)\hat{a}_y \quad (3)$$

(10 Marks)

(c) In free space ($z \leq 0$), a plane wave with an electric filed (V/m) given by equation (4) is incident normally on a lossless medium ($\epsilon = 2\epsilon_0$, $\mu = 8\mu_0$) in region $z \geq 0$. Determine the reflected wave, $\vec{H}_r$ and $\vec{E}_r$. [Use figure 2 to aid your calculations.]

$$\vec{E}_i = 10cos(10^8 t - \beta z)\hat{a}_x \quad (4)$$

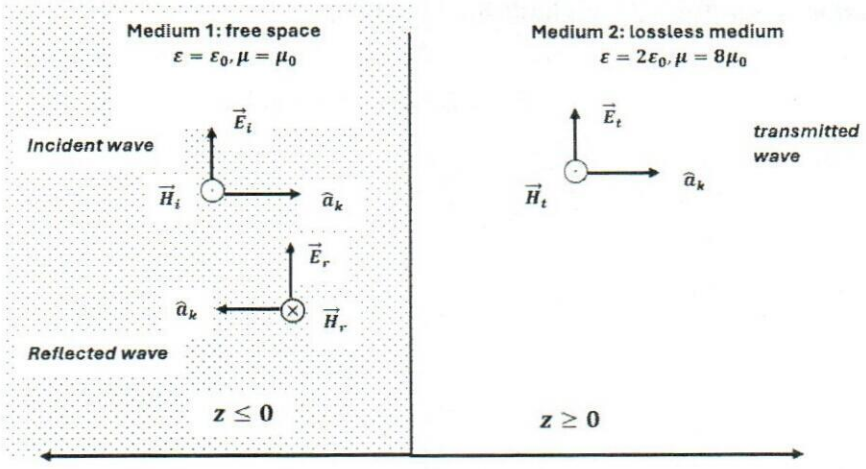

Figure 2

(10 Marks)

[Total - 25 Marks]

Question 04

(a) Wave polarization is the orientation of oscillation of the electric field in an electromagnetic wave. Determine the type of polarization of the wave given in equation (5).

$$\vec{E}(z,t) = 3e^{-0.75z}sin(10^8t - z)\hat{a}_x + 4e^{-0.75z}cos(10^8t - z)\hat{a}_y \quad (5)$$

(05 Marks)

(b) Guided wave transmission refers to the propagation of waves along a specific structure that confines wave energy and directs it. Compare and contrast two of the guided wave transmission methods of electromagnetic waves namely, waveguides and transmission lines. [Give 03 differences]

(06 Marks)

(c) In an air-filled waveguide as shown in Figure 3, the cutoff frequency of a TE_{10} mode is $5GHz$, whereas that of a TE_{01} mode is $12GHz$. Calculate,

(i) The dimensions of the guide, $a(cm)$ and $b(cm)$.

(ii) The cutoff frequencies of the next three higher TE modes.

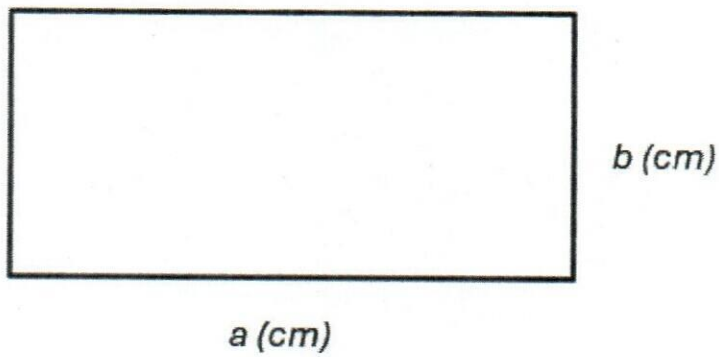

Figure 3

(14 Marks)

[Total - 25 Marks]

FORMULA SHEET

Electrostatics:

Total line charge,

$$Q = \int_{z_A}^{z_B} \rho_L \, dz$$

Laplace's Equation and Poisson's equation,

$$\nabla^2 V = 0 \;\; ; \;\; \nabla^2 V = -\frac{\rho_v}{\varepsilon}$$

Time-harmonic fields:

Phasor form of $\vec{A} = A_0 \cos(\omega t - \beta x)\hat{a}_y$,

$$\vec{A}(x,y,z,t) = \Re\left[\vec{A}_s(x,y,z)e^{j\omega t}\right] where, \;\; ; \;\; \vec{A}_s = A_0 e^{-j\beta x}\hat{a}_y$$

Faraday's law,

$$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t}; \vec{B} = \mu\vec{H} \quad \Rightarrow \quad \vec{B} = -\frac{1}{\mu}\int (\nabla \times \vec{E})\, dt$$

Ampere's law,

$$\nabla \times \vec{H} = \sigma\vec{E} + \varepsilon\frac{\partial \vec{E}}{\partial t} \quad \Rightarrow \quad \vec{E} = -\frac{1}{\varepsilon}\int (\nabla \times \vec{H})\, dt$$

Wave propagation:

Phase constant,

$$\beta = \frac{2\pi}{\lambda} = \frac{\omega}{u}$$

Wave propagation in good conductors,

$$\alpha = \beta = \sqrt{\frac{\mu\omega\sigma}{2}} \;\; ; \;\; |\eta| = \sqrt{\frac{\mu\omega}{\sigma}} \;\; ; \;\; \tan 2\theta_\eta = \frac{\sigma}{\omega\varepsilon} \;\; ; \;\; H_0 = \frac{E_0}{|\eta|} \;\; ; \;\; \hat{a}_H = \hat{a}_k \times \hat{a}_E$$

Incident, reflected and transmitted waves in phasor form,

$$\vec{E}_{is}(z) = E_{i0}e^{-\gamma z}\hat{a}_x \;\; ; \;\; \vec{E}_{rs}(z) = E_{r0}e^{\gamma z}\hat{a}_x \;\; ; \;\; \vec{E}_{ts}(z) = E_{t0}e^{-\gamma z}\hat{a}_x$$

Reflection coefficient,

$$\Gamma = \frac{E_{r0}}{E_{i0}} = \frac{\eta_2 - \eta_1}{\eta_2 + \eta_1}$$

Guided wave transmission:

$$f_c = \frac{u'}{2}\sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{n}{b}\right)^2} \;\; ; \;\; u' = \frac{1}{\sqrt{\mu\varepsilon}} \;\; ; \;\; \eta = \frac{\eta'}{\sqrt{1 - \left(\frac{f_c}{f}\right)^2}} \;\; ; \;\; \eta' = \sqrt{\frac{\mu}{\varepsilon}}$$

Important constants:

$$\mu_0 = 4\pi \times 10^{-7} H/m \;\; ; \;\; \epsilon_0 = \frac{10^{-9}}{36\pi} = 8.85 \times 10^{-12} F/m \;\; ; \;\; c = 3 \times 10^8 m/s$$

-END OF EXAMINATION PAPER-

CINEC CAMPUS
Beyond A Graduate

CINEC Campus
Faculty of Engineering and Technology
Department of Electrical and Electronics Engineering
BSc Hons (Eng) Electronic and Telecommunication Engineering
Semester 05 First-Sit Examination 2025

Module Code	**: EE3318**
Module Title	**: Computer Networks**
Date	**: 27th January 2025**
Examiners	**: Dr. Samiru Gayan**
Time Allowed	**: 9.00 AM – 12.00 PM, 3 hours**

INSTRUCTIONS TO CANDIDATES

- This is a **closed book** examination.
- You should answer **ALL** questions.
- Write clearly legibly with a blue or black pen.
- Use only the **CINEC answering booklet.** Additional sheets may be requested from the invigilators.
- This paper consists of **six** pages.

MATERIALS REQUIRED

- CINEC answering booklet with extra answering papers.
- You may use a scientific calculator. This must not be programmable. This may be examined during the examination.

Question 1

(a) Match the following to one or more layers of the OSI model:

(i) Reliable process-to-process message delivery (1 mark)

(ii) Route selection (1 mark)

(iii) Defines frames (1 mark)

(iv) Provides user services such as e-mail and file transfer (1 mark)

(v) Transmission of bit stream across the physical medium (1 mark)

(b) For each of the following four networks, discuss the consequences if a connection fails.

(i) Five devices arranged in a mesh topology. (2 marks)

(ii) Five devices arranged in a star topology (not counting the hub). (2 marks)

(iii) Five devices arranged in a bus topology. (2 marks)

(iv) Five devices arranged in a ring topology. (2 marks)

(c) Suppose a computer sends a frame to another computer on a bus topology LAN. The physical destination address of the frame is corrupted during the transmission. What happens to the frame? How can the sender be informed about the situation?

(4 marks)

(d) Suppose a computer sends a packet at the network layer to another computer somewhere on the Internet. The logical destination address of the packet is corrupted. What happens to the packet? How can the source computer be informed of the situation?

(4 marks)

(e) If the data link layer can detect errors between hops, why do you think we need another checking mechanism at the transport layer?

(4 marks)

Total [25 marks]

Question 2

(a) What is the significance of the twisting in twisted-pair cable? (2 marks)

(b) Draw the graph of the NRZ-L and NRZ-I schemes for the following data streams, assuming that the last signal level has been positive.

(i) 01010101 (4 marks)

(ii) 00110011 (4 marks)

(c) A path in a digital circuit-switched network has a data rate of 1 Mbps. The exchange of 1000 bits is required for the setup and teardown phases. The distance between the two parties is 5000 km. Answer the following questions if the propagation speed is 2×10^8 ms^{-1}:

(i) What is the total delay if 1000 bits of data are exchanged during the data transfer phase?

(3 marks)

(ii) What is the total delay if 100,000 bits of data are exchanged during the data transfer phase?

(3 marks)

(iii) Find the delay per 1000 bits of data for each of the above cases and compare them. What can you infer?

(3 marks)

(d) Transmission of information in any network involves end-to-end addressing and sometimes local addressing. Answer the following questions:

(i) Why does a circuit-switched network need end-to-end addressing during the setup and teardown phases? Why are no addresses needed during the data transfer phase for this type of network?

(3 marks)

(ii) Why does a datagram network need only end-to-end addressing during the data transfer phase, but no addressing during the setup and teardown phases?

(3 marks)

Total [25 marks]

Question 3

(a) Define controlled access and list three protocols in this category. (3 marks)

(b) What is the purpose of a Network Interface Card (NIC)?

(3 marks)

(c) Answer the following questions on Ethernet.

(i) How does the Ethernet address 1A:2B:3C:AD:5E:6F appear on the line in binary?

(2 marks)

(ii) If an Ethernet destination address is 07:01:02:03:04:05, what is the type of the address (unicast, multicast, or broadcast)?

(2 marks)

(iii) The address 43:7B:6C:DE: 10:00 has been shown as the source address in an Ethernet frame. The receiver has discarded the frame. Why?

(3 marks)

(iv) An Ethernet MAC sublayer receives 42 bytes of data from the upper layer. How many bytes of padding must be added to the data?

(3 marks)

(v) An Ethernet MAC sublayer receives 1510 bytes of data from the upper layer. Can the data be encapsulated in one frame? If not, how many frames need to be sent? What is the size of the data in each frame?

(3 marks)

(d) There are some useful parameters in local area networks (LANs) to get deeper insights into their quality.

(a) One of such useful parameters in a LAN is the number of bits that can fit in one meter of the medium ($n_{b/m}$). Find the value of $n_{b/m}$ if the data rate is 100 Mbps and the medium propagation speed is 2×10^8 m/s.

(2 marks)

(b) Another useful parameter in a LAN is the bit length of the medium (L_b), which defines the number of bits that the medium can hold at any time. Find the bit length of a LAN if the data rate is 100 Mbps and the medium length in meters (L_m) for communication between two stations is 200 m. Assume the propagation speed in the medium is 2×10^8 m/s.

(2 marks)

(c) We define the parameter γ as the number of frames that can fit the medium between two stations. Derive an equation for γ in terms of L_b and the frame length of the medium F_b.

(2 marks)

Total [25 marks]

Question 4

(a) Briefly describe three *advantages* and three *disadvantages* of optical fiber over twisted-pair and coaxial cable. (6 marks)

(b) Network designers generally attempt to deploy networks that don't have single points of failure, though they don't always succeed. Network topologies that employ redundancy are of much interest.

(i) Draw an example of a six-node network in which the failure of a single link does not disconnect the entire network (that is, any node can still reach any other node).

(3 marks)

(ii) Draw an example of a six-node network in which the failure of any single link cannot disconnect the entire network, but the failure of some single node does disconnect it.

(3 marks)

(iii) Draw an example of a six-node network in which the failure of any single node cannot disconnect the entire network, but the failure of some single link does disconnect it.

(3 marks)

Note: Not all the cases above may have a feasible example.

(c) An organization is granted the block 211.17.180.0/24. The administrator wants to create 32 subnets.

(i) Find the subnet mask. (2 marks)

(ii) Find the number of addresses in each subnet. (2 marks)

(iii) Find the first and last addresses in subnet 1. (2 marks)

(iv) Find the first and last addresses in subnet 32. (2 marks)

(d) Why do Open Shortest Path First (OSPF) messages propagate faster than Routing Information Protocol (RIP) messages? (2 marks)

Total [25 marks]

- End of Question Paper -

CINEC CAMPUS
Beyond A Graduate

CINEC Campus
Faculty of Engineering & Technology
Department of Electrical & Electronic Engineering
BSc Hons (Eng) Electronic and Telecommunication Engineering
Semester 05 First-Sit Examination 2025

Module Code	:	**EE3315**
Module Title	:	**Digital Systems Design**
Date	:	**2025.01.25**
Examiners	:	**Athula Seneviratne**
Time Allowed	:	**1:30 PM – 4:30 PM; 03 hrs**

INSTRUCTIONS TO CANDIDATES

- This is a **closed book** examination.
- This paper consists of two parts. Both parts must be answered:
  - **Part 'A'** contains forty (40) questions of the Multiple-Choice type. **All** questions carry **equal** marks. You should answer **ALL** questions.
  - **Part 'B'** contains two (02) descriptive type questions. Both questions carry equal marks. You should answer **BOTH** questions.
- Mark/Write your answers clearly and legibly with a **blue** or **black** pen.
- Use only the **MCQ Answering Sheet** provided to answer Part 'A' and only the **CINEC Answering Booklet** to answer Part 'B'. Additional sheets may be requested from the invigilators.
- This paper contains twelve (12) pages including this page.
- All papers used to perform rough work / draft calculations must be attached to the answer sheet and submitted.

MATERIAL REQURIED

- MCQ Answering Sheet, CINEC Answering Booklet, and paper for carrying out rough work.
- You may use a scientific calculator. This must not be programmable. This may be examined during the examination.

Part 'A'

This part contains 40 multiple-choice questions. Each question has 4 answers. You are required to select the **most correct** answer for each question and indicate it on the answer sheet provided, by marking a cross (X) across the selected number of the answer.

[Each multiple-choice question carries 1 mark]

01 Hardware Description Languages (HDL) are used to
   a. define computations at hardware level
   b. generate machine code for a given processor
   c. design sequential circuits
   d. design and simulate hardware systems

02 To what level of resource hierarchy does a Field Programmable Gate Array (FPGA) belong?
   a. Configware
   b. Firmware
   c. Hardware
   d. System software

03 Which of the following best matches with the concept of 'reconfigurable computing'?
   a. Both resources and algorithms are variable
   b. Resources variable, algorithms fixed
   c. Resources fixed, algorithms variable
   d. Both resources and algorithms are fixed

04 What is the purpose served by a Place and Route (PnR) map?
   a. Defines the outputs generated by each combination of input values
   b. Describes the detailed layout and interconnections between all physical components
   c. Defines the nodes to which each physical component must be connected
   d. Defines the signal flow between physical components

05 What is the purpose served by a Netlist?
   a. Defines the outputs generated by each combination of input values
   b. Describes the detailed layout and interconnections between all physical components
   c. Defines the nodes to which each physical component must be connected
   d. Defines the signal flow between physical components

06 What is the end product of a correctly compiled HDL program?
   a. Simulation file
   b. Netlist
   c. PnR map
   d. None of the above

Refer to the VHDL script given in Figure 1, to answer questions 07 and 08:

```
-- Start of script "Four-bitRCAdder.vhd"
-- Import the necessary libraries
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Define the entity 'Four_bitRCAdder'
entity Four_bitRCAdder is
    port(
    A, B     : in STD_LOGIC_VECTOR(7 downto 0);
    Cin      : in STD_LOGIC;

    S        : out STD_LOGIC_VECTOR(7 downto 0);
    Cout     : out STD_LOGIC
    );
end Four_bitRCAdder;

-- Define the architecture for the entity 'Four_bitRCAdder'
architecture AdderBehavio of Four_bitRCAdder is
    -- Define the internal signals
    signal C1, C2, C3, C4, C5, C6, C7    : STD_LOGIC;

begin
    FA0: entity work.FullAdder port map (A(0), B(0), Cin, S(0), C1);
    FA1: entity work.FullAdder port map (A(1), B(1), C1, S(1), C2);
    FA2: entity work.FullAdder port map (A(2), B(2), C2, S(2), C3);
    FA3: entity work.FullAdder port map (A(3), B(3), C3, S(3), C4);
    FA4: entity work.FullAdder port map (A(4), B(4), C4, S(4), C5);
    FA5: entity work.FullAdder port map (A(5), B(5), C5, S(5), C6);
    FA6: entity work.FullAdder port map (A(6), B(6), C6, S(6), C7);
    FA7: entity work.FullAdder port map (A(7), B(7), C7, S(7), Cout);
end AdderBehavio;
-- End of script "Four_bitRCAdder.vhd"
```

Figure - 1

07 What is the size of the variable '**S**' in the entity called '**Four_bitRCAdder**'?
   a. 4 bits
   b. 6 bits
   c. 7 bits
   d. 8 bits

08 What is the name of the entity that is **not** defined in the script "**Four-bitRCAdder.vhd**"?
   a. FullAdder
   b. Four-bitRCAdder
   c. Library IEEE
   d. work.FullAdder

```
37
38  W <= A and B and C
39
40  X <= A xor C or B
41
42  Y <= A nor W
43
44  Z <= not (C and X)
45
```

Figure - 2

09 Figure – 2 shows 4 lines in a VHDL script. What are the lines that will be concurrently executed whenever the value of variable 'B' changes?
   a. Line 38 only
   b. Line 38 and 40 only
   c. All 4 lines 38, 40, 42, and 44
   d. None of the 4 lines 38, 40, 42, or 44

10 Which of the following statement is **incorrect** about a 'register' in computer hardware?
   a. It is a storage unit of fixed size
   b. It has an access time greater than that of RAM
   c. The value stored in a register defines its 'state'
   d. Each bit may be accessed for operations

11 When performing circuit design using a Register Transfer Language (RTL), the designer defines
   a. how a clock should be applied to the circuit
   b. how and when data should flow between registers
   c. how centralized control may be achieved using a processor
   d. how the circuit should be implemented at hardware level

12 The part of the Instruction Register (IR) that provides inputs to the Control Unit of the processor is called
   a. address field
   b. data field
   c. operand field
   d. opcode field

13 The purpose of the 'Flag Register' in a processor is to
   a. Indicate various outcomes of the last operation performed
   b. Indicate that the last operation generated a carry
   c. Indicate that all registers are full
   d. Indicate that the processor temperature is high

14 The difference between a 'compiler' and an 'assembler' mainly lies in their
   a. sizes
   b. Associated processors
   c. outputs
   d. Input sources

15 A disadvantage of using centralized control is
   a. All control signals may be synchronized
   b. All inputs may be coordinated
   c. It results in a single point of failure
   d. None of the above

16 Which of the following is a technique used for low power processor design?
   a. Power islands
   b. pipelining
   c. Clock gating
   d. All of the above

17 Choose the **incorrect** statement
   a. When using RTL, design is done at 'high-level'
   b. RTL are 'how to do' languages
   c. Dataflow between entities defined by RTL coding
   d. Architecture of entities is defined by RTL coding

18 What is the technique used to alter the normal sequence of execution of a program stored in the memory?
   a. Input/output
   b. Register windowing
   c. Interrupts
   d. Clock gating

19 The instruction format of a microprocessor uses a 5-bit opcode field. What is the maximum number of independent instructions the processor can support?
   a. 32
   b. 16
   c. 8
   d. 5

20 Choose the **correct** statement about CISC processors
   a. They support only a few addressing modes
   b. They internally cache 'instructions and 'data' separately
   c. Only a few instructions can be used for memory access
   d. Machine level program size is small

21 What is the reason for compilers of RISC processors to be large in size and comprehensive in operation?
   a. An RISC processor has a large number of registers for storing variables at runtime
   b. They take over the load of producing machine code for complex computations using a small instruction set
   c. RISC processors have short machine cycles and therefore requires larger number of steps
   d. The machine level program size is small in RISC processor based systems

22 Which of the following is **not necessarily** a characteristic of an RISC processor?
   a. High speed
   b. Low power consumption
   c. Large register file
   d. Small instruction set

```
A[1] := SQUARE(X) + FACTORIAL(X)/ SQUARE(Z)

A[2] := FACTORIAL(W) + FACTORIAL(Z)

A[3] := SQUARE(Y) + 3*X
```

Figure – 3

Figure – 3 shows 3 consecutive lines of a main program written in a high-level language. It calls two functions. One function computes the factorial of an integer passed to it while the other function computes the square of an integer passed to it. This program is compiled for execution in a computing machine that uses an RISC processor having 48 registers. The compiler assigns registers to variables in the program in the manner shown in Figure - 4.

23 What is the register that is **most likely** to store the variable 'X' during program execution?
   a. R5
   b. R10
   c. R23
   d. R35

24 What is the register that is **most likely** to store the variable 'Z' during program execution?
   a. R5
   b. R10
   c. R23
   d. R35

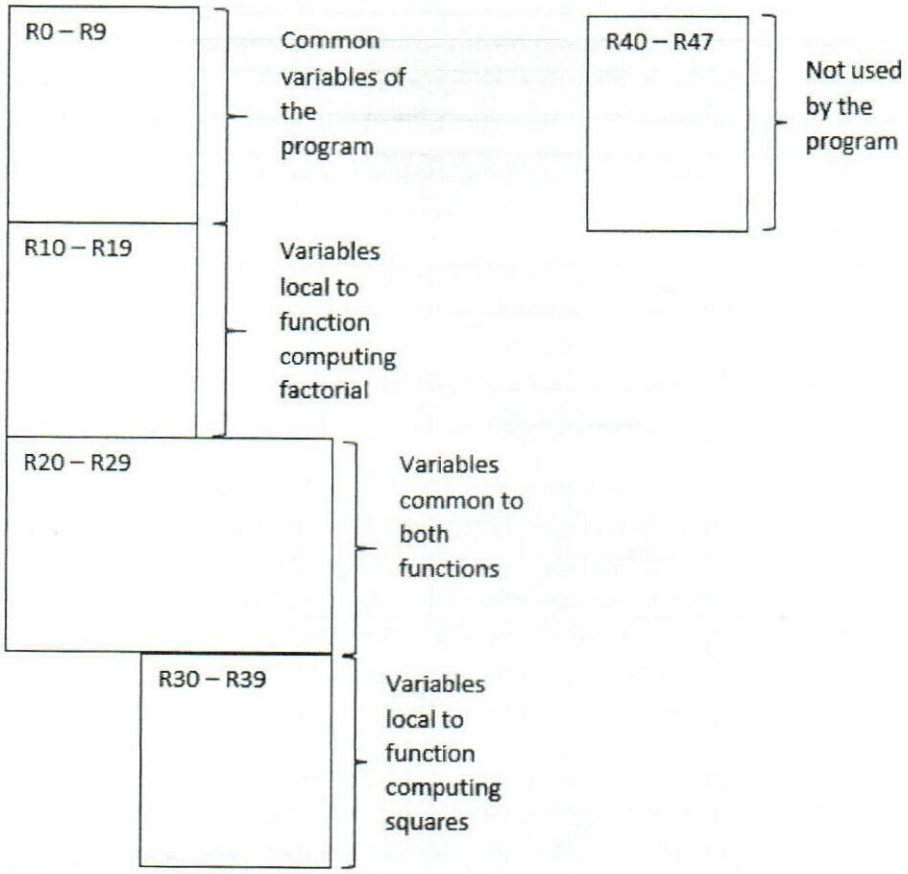

Figure – 4

25 What is the register that is **most likely** to store the variable 'Y' during program execution?
   a. R5
   b. R10
   c. R23
   d. R35

26 What is the technique used in an RISC processor as illustrated in Figure – 4 called?
   a. Register mapping
   b. Register organization
   c. Register re-naming
   d. Register windowing

27 Which of the following systems/devices is **most likely** to use an RISC processor?
   a. Router
   b. Desktop
   c. Smartphone
   d. Server

28 Choose the **incorrect** statement
   a. Contents of the RWM are lost when power is switched off
   b. The RAM is external to the microprocessor
   c. Both address bus and data bus run between the microprocessor and the RAM
   d. The onboard ROM is not a part of the RAM

29 In microprocessor based systems, **cache memory** is used to
   a. increase overall memory capacity
   b. speed up programme execution
   c. backup the RAM at the end of each machine cycle
   d. store data when RAM overflows

30 Choose the list of memory devices arranged in the order of increasing speed, left to right
   a. Regular RAM, external cache, level-1 cache, registers
   b. Regular RAM, external cache, level-1 cache, level-2 cache
   c. Regular RAM, registers, level-2 cache, external cache
   d. Regular RAM, external cache, registers, level-2 cache

31 Choose the list of memory devices arranged in the order of increasing capacity, left to right
   a. Regular RAM, external cache, level-2 cache, level-1 cache
   b. Level-1 cache, external cache, level-2 cache, regular RAM
   c. Level-1 cache, level-2 cache, external cache, regular RAM
   d. External cache, level-2 cache, level-1 cache, regular RAM

32 How many data pins are there in a single dynamic RAM chip?
   a. 16
   b. 8
   c. 1
   d. None of the above

Figure-5 shows the schematic of a 1-bit memory cell

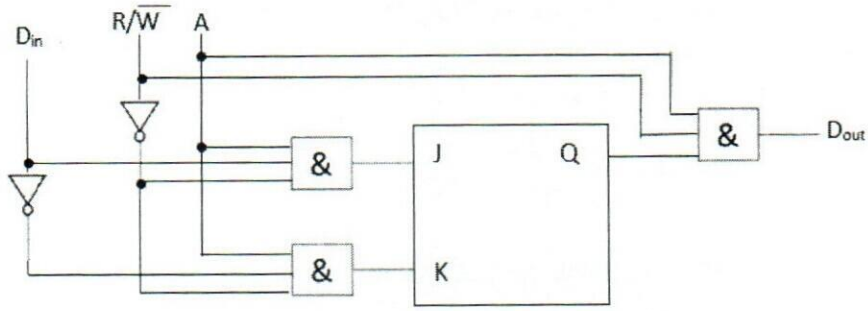

Figure - 5

33 Purpose of input 'A' is to
a. select memory write operation
b. select the memory cell
c. select memory read operation
d. do none of the above

34 To write to the memory cell
a. 'A' must be enabled, R/$\overline{W}$ must be set to '1', Data must be placed at D_{in}
b. 'A' must be enabled, R/ $\overline{W}$ must be set to '0', Data must be placed at D_{in}
c. 'A' must be enabled, R/$\overline{W}$ must be set to '0', Data must be placed at D_{out}
d. 'A' must be disabled, R/$\overline{W}$ must be set to '1', Data must be placed at D_{in}

35 A dynamic RAM chip is of capacity 4096 x 1. How many address pins does it have?
a. 1
b. 4
c. 8
d. 12

36 When designing a 4096 x 1 RAM chip using VHDL, what is the entity that is most suitable to be selected as the building block?
a. 1-bit memory cell
b. JK flip flop
c. NAND gate
d. NOR gate

37 In asynchronous sequential circuits
a. there is no clock input
b. there are no flip flops
c. the clock input is controlled by an external event
d. the circuit does not possess any memory

38 Which of the following is a practical example of an asynchronous system?
a. Microprocessor of the RISC type
b. People counter in an isle
c. Multi display clock
d. User programmable sequence generator

39 When designing sequential systems using VHDL, the order of execution of statements as listed in the program is **forced** by using
a. '**entity**' statements
b. '**architecture**' statements
c. '**signal**' definitions
d. '**process**' statements

40 In VDL development packages, a **functional simulator** is provided for
   a. checking the designed circuit for correct operation, disregarding the delays in the individual circuit elements
   b. checking the designed circuit for correct operation, taking the delays in the individual circuit elements into account
   c. producing the 'Netlist' for the circuit at logic gate and flipflop level
   d. producing the list at resister, transistor level

Part 'B'

Question '1'

It is required to design a 3-bit binary comparator whose output 'Z' is logic '1' if and only if the two binary inputs $a_2a_1a_0$ and $b_2b_1b_0$ are numerically equal to each other (i.e. each corresponding bit is equal), and is logic '0' for all other input combinations.

(i) Using first principles, show that a 2-input X-NOR gate performs the function of a 1-bit comparator.

[5 marks]

(ii) By intuition, draw a simple combinational circuit that uses 2-input X-NOR gates and any other required combinational logic components, to realize a 3-bit binary comparator as specified above. Clearly label all intermediate signals.

[5 marks]

(iii) Assume that an entity which implements a 2-input X-NOR gate has been written in VHDL and is available in compiled form under the name 'EXNOR' which can be readily used in a VHDL script. Write the VHDL code for the entity and the architecture that would implement your circuit drawn for 'ii' above, making use of the entity EXNOR. (Library import statements are not required. You must use the same labels that you used for the intermediate signals when defining any internal signals for the architecture. Good coding practice that ensures readability is expected).

[15 marks]

(iv) The VHDL script for the 3-bit comparator is to be tested for proper operation using 'functional simulation'. If the waveform editor of the simulator application has a default grid size of 10 ns, calculate the minimum duration of the input waveforms that are required to test the comparator for its full functionality.
(***Hint:*** *Testing a circuit for full functionality means testing with all possible input combinations*)

[5 marks]

Question '2'

Figure – 6 indicates the schematic diagram for a 3-bit event counter that uses three (03) T-flip-flops (toggle flip-flops). The clock input (ϕ) is driven by a pulse shaper that is triggered by the external event that is intended to be counted.

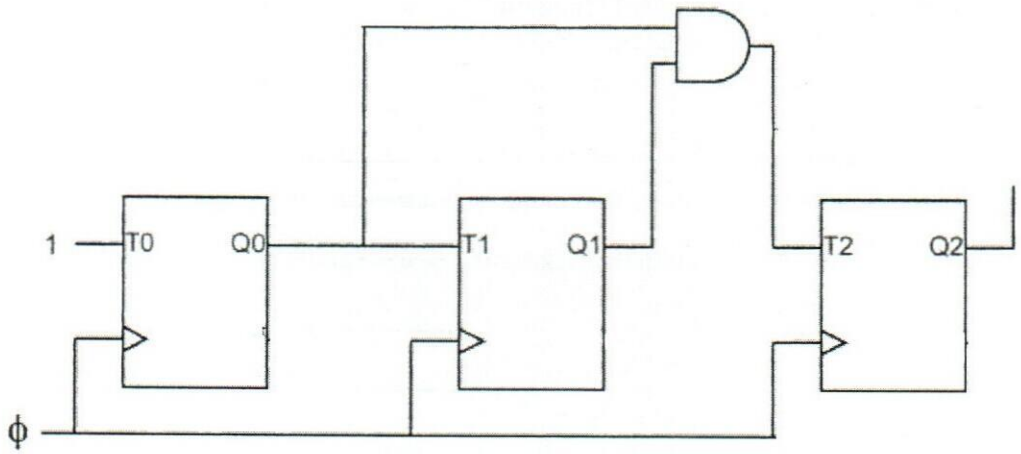

Figure - 6

(i) The VHDL code given in Figure – 7 implements a T-flip-flop. Identify two errors in the script that would prevent its successful compilation. You may indicate the line number and describe the error. ***[10 marks]***

```
6   library IEEE;
7   use IEEE.STD_LOGIC_1164.ALL;
8
9   entity TFF is
10      port (T, phy:  in STD_LOGIC; -- inputs  ('phy' is the clock input)
11            Q: out STD_LOGIC;  -- Q output
12            Qbar: out STD_LOGIC := '1' -- (complement of Q)
13            );
14            -- Q becomes '0' by default. So Qbar is forced to '1'
15  end TFF;
16
17
18
19  architecture T_FF_Behavior of T_FF is
20
21      signal Q_val: std_logic;
22      signal Q_next: std_logic;
23  begin
24      Q_next <= NOT Q_val when(T='1' ) else
25                Q_val;
26      Q <= Q_next;
27      Qbar <= not Q_val;
28
29      process(phy)
30      begin
31          if (phy='1') then
32              Q_val <= Q_next;
33          end if
34      end process;
35
36  end T_FF_Behavior;
```

Figure - 7

(ii) Write the VHDL code for an '**entity – architecture pair**' to implement the 3-bit event counter given in Figure – 6, using the entity 'TFF' given in the script of Figure – 7 as a building block and appropriate 'port mapping' (Library import statements are not required. Good coding practice that ensures readability is expected).

[15 marks]

(iii) Describe one (01) basic difference between 'Hardware Description Languages' and other conventional high-level programming languages.

[5 marks]

- End of Examination Paper -

Library.

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CINEC CAMPUS
Beyond A Graduate

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Answer sheet for answering multiple choice questions

Each question in the question paper has 4 answers. You are required to select the **most correct** answer for each question and indicate it on the answer sheet provided, by marking a cross (X) across the selected number of the answer.

Kindly **mark only one (01) answer** for **each** question. Zero marks will be awarded for any question for which more than one (01) answer is marked.

(1)	a	b	c	d	(21)	a	b	c	d
(2)	a	b	c	d	(22)	a	b	c	d
(3)	a	b	c	d	(23)	a	b	c	d
(4)	a	b	c	d	(24)	a	b	c	d
(5)	a	b	c	d	(25)	a	b	c	d
(6)	a	b	c	d	(26)	a	b	c	d
(7)	a	b	c	d	(27)	a	b	c	d
(8)	a	b	c	d	(28)	a	b	c	d
(9)	a	b	c	d	(29)	a	b	c	d
(10)	a	b	c	d	(30)	a	b	c	d
(11)	a	b	c	d	(31)	a	b	c	d
(12)	a	b	c	d	(32)	a	b	c	d
(13)	a	b	c	d	(33)	a	b	c	d
(14)	a	b	c	d	(34)	a	b	c	d
(15)	a	b	c	d	(35)	a	b	c	d
(16)	a	b	c	d	(36)	a	b	c	d
(17)	a	b	c	d	(37)	a	b	c	d
(18)	a	b	c	d	(38)	a	b	c	d
(19)	a	b	c	d	(39)	a	b	c	d
(20)	a	b	c	d	(40)	a	b	c	d